EE 435

Lecture 31

String DACs

DAC Architectures (Nyquist Rate)

Types

- Voltage Scaling
  - Resistor String DACs (string DACs)
  - Interpolating
- Current Steering
  - Binarily Weighted Resistors
  - R-2R Ladders
  - Current Source Steering
    - Thermometer Coded
    - Binary Weighted
    - Segmented
- Charge Redistribution
  - Switched Capacitor
- Serial
  - Algorithmic
  - Cyclic or Re-circulating
  - Pipelined
- Integrating
- Resistor Switching
- MDACs (multiplying DACs)

DAC Architectures

Structures

- Hybrid or Segmented
- Mode of Operation
  - Current Mode
  - Voltage Mode
  - Charge Mode
- Self-Calibrating
  - Analog Calibration
    - Foreground
    - Background
  - Digital Calibration
    - Foreground
    - Background
  - Dynamic Element Matching
- Laser of Link Trimmed
- Thermometer Coded or Binary
- Radix 2 or non-radix 2
- Inherently Monotone

DAC Architectures

- Type of Classification may not be unique nor mutually exclusive
- Structure is not mutually exclusive
- All approaches listed are used (and probably some others as well)
- Some are much more popular than others
  - Popular Architectures
    - Resistor String (interpolating)
    - Current Source Steering (with segmentation)
- Many new architectures are possible and some may be much better than the best currently available
- All have perfect performance if parasitic and matching performance are ignored !
- Major challenge is in determining appropriate architecture and managing the parasitics

Nonideal Effects of Concern

- Matching
- Parasitic Capacitances
  (including Charge injection)
- Loading
- Nonlinearities
- Previous code dependence
- Code-dependent settling
- Interconnect resistors
- Noise
- Slow and plagued by jitter
- Temperature Effects
- Aging
- Package stress

Observations

- Yield Loss is the major penalty for not appropriately managing parasitics and matching and this loss can be ruthless
- The ultimate performance limit of essentially all DACs is the yield loss associated with parasitics and matching
- Many designers do not have or use good statistical models that accurately predict data converter performance
- If you work of a company that does not have good statistical device models
  - Convince model groups of the importantc of dedveloping these models
  - (or) develop appropriate test strutures to characterize your process
- Existing nonlinear device models may not sufficiently accurately predict device nonlinearities for high-end data converter applications

Observations

- Experienced Designers/Companies often produce superior data converter products
- Essentially all companies have access to the same literature, regularly reverse engineer successful competitors products and key benefits in successful competitors products are generally not locked up in patents
- High-end designs(speed and resolution) may get attention in the peer community but practical moderate performance converters usually make the cash flow
- Area (from a silicon cost viewpoint) is usually not the driving factor in high-end designs where attractive price/mfg cost ratios prevail

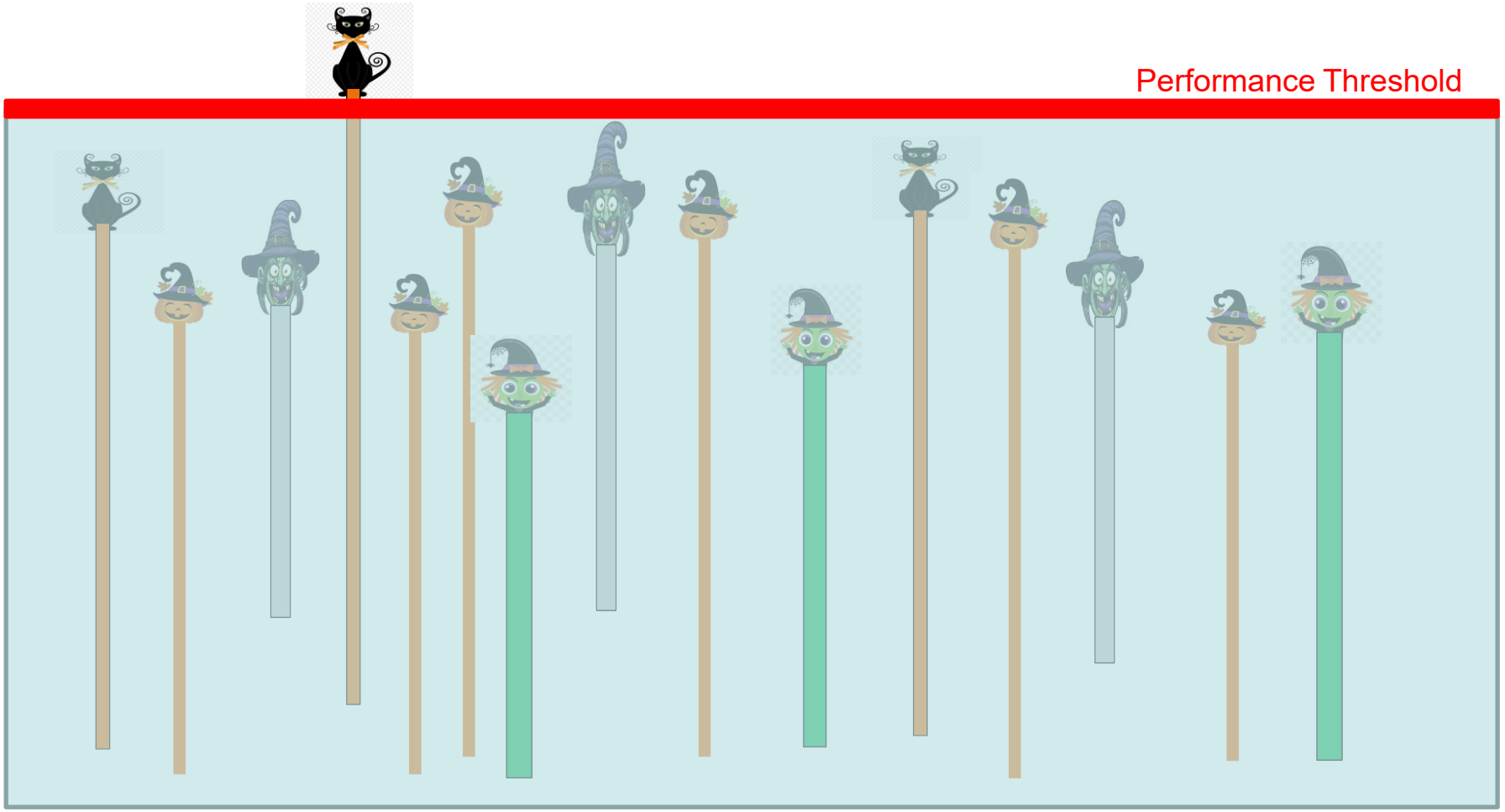
Data Converter Design Strategies

- There are many different DAC and ADC architectures that have been proposed and that are in widespread use today
- Almost all work perfectly if all components are ideal
- Most data converter design work involves identifying the contributors to nonideal performance and finding work-arounds to these problems
- Some architectures are more difficult to find work-arounds than others
- All contributors to nonidealities that are problematic at a given resolution of speed level must be identified and mitigated
- The effects of not identifying nonidealities generally fall into one of two categories
  - Matching-critical nonidealities (degrade yield)
  - Component nonlinearities (degrade performance even if desired matching is present)

Data Converter Design Strategies

Remember:

Need to keep nonideal effects below an acceptable performance threshold



Identifying Problems/Challenges and Clever/Viable Solutions

- Many problems occur repeatedly so should recognize when they occur
- Identify clever solutions to basic problems – they often are useful in many applications
- Don't make the same mistake twice !

The problem:

The perceived solution:

The practical or clever solution:

Keep A List !

Identifying Problems/Challenges and Clever/Viable Solutions

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The problem:

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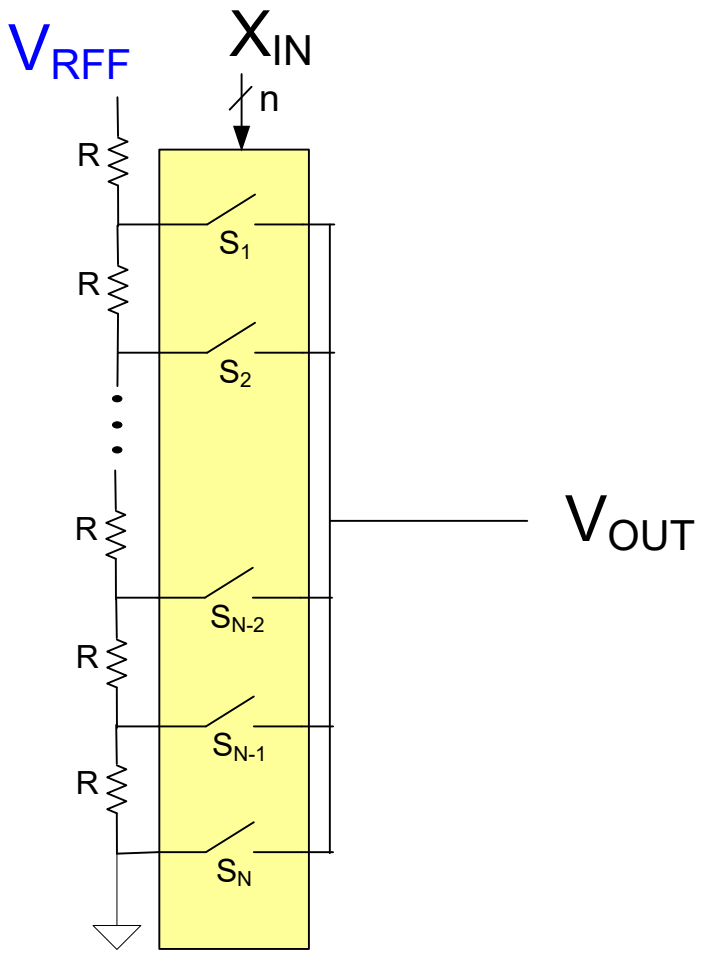
The practical or clever solution:

The List !

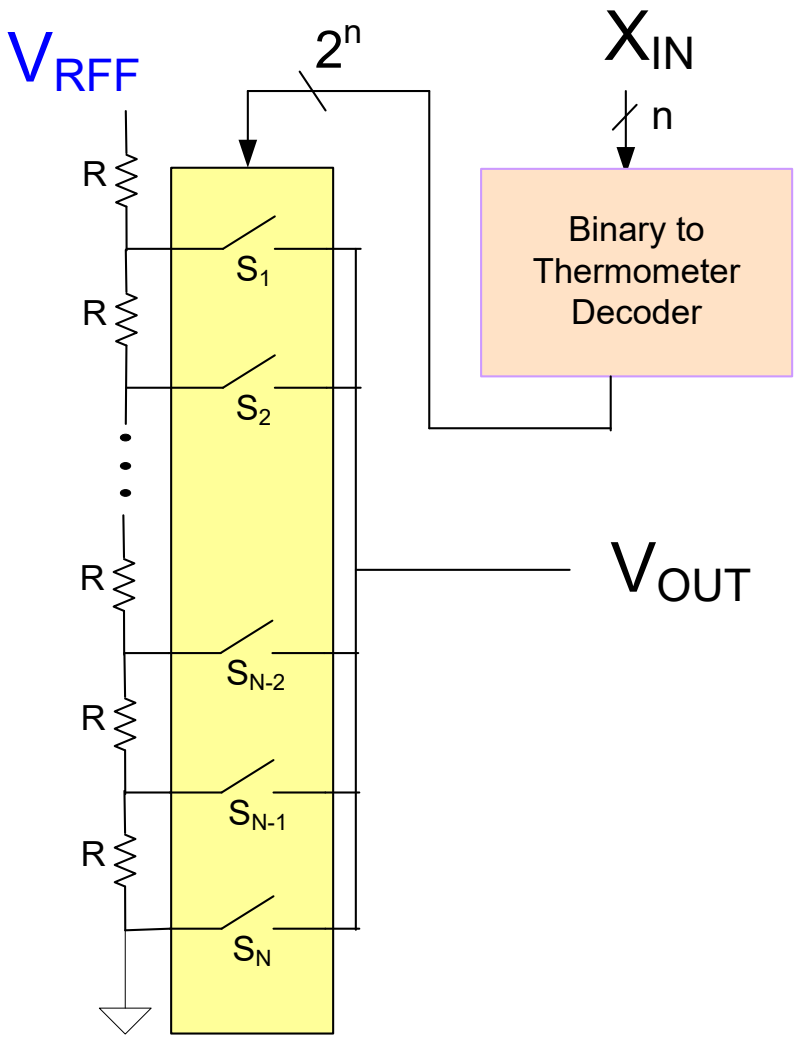
The List Keeper !

R-String DAC



Basic R-String DAC

R-String DAC



Basic R-String DAC including Logic to Control Switches

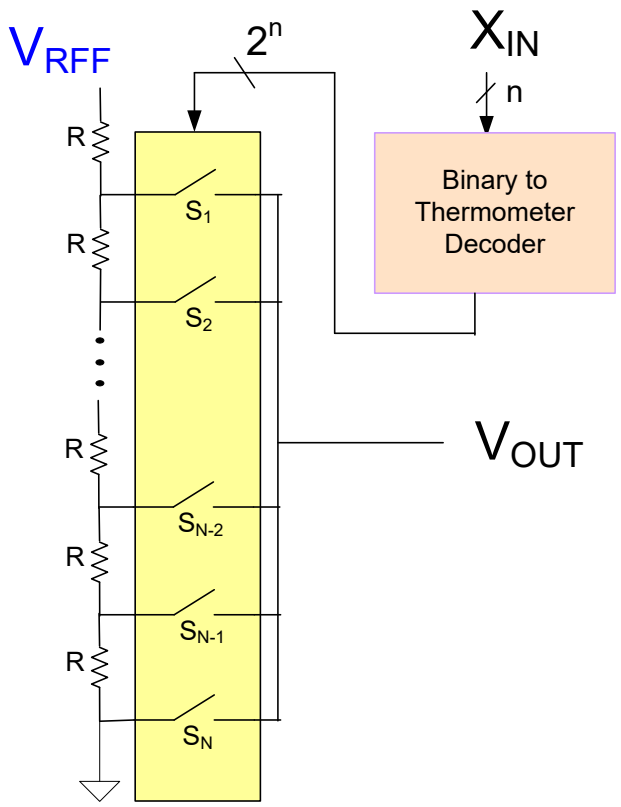
R-String DAC

If all components are ideal, performance of the R-string DAC is that of an ideal DAC!

Key Properties of R-String DAC

- One of the simplest DAC architectures
- R-string DAC is inherently monotone

Possible Limitations or Challenges



R-String DAC

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Key Properties of R-String DAC

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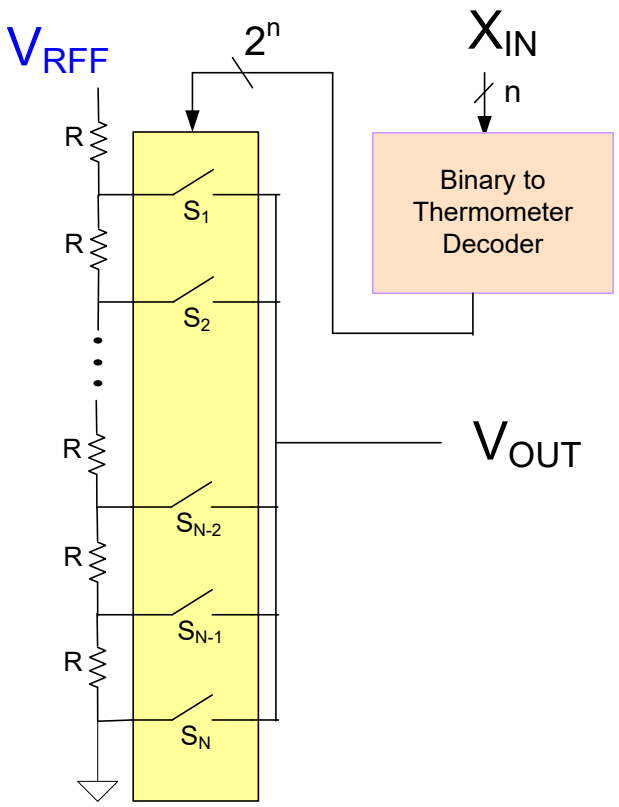
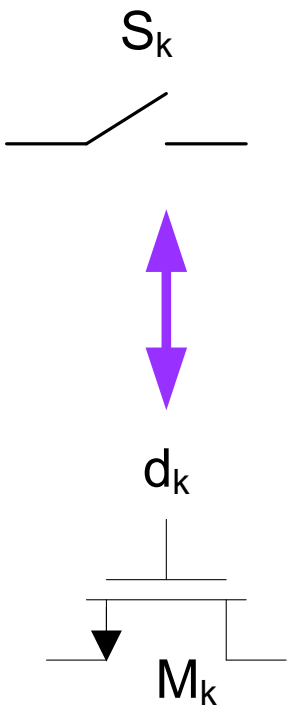
Possible Limitations or Challenges

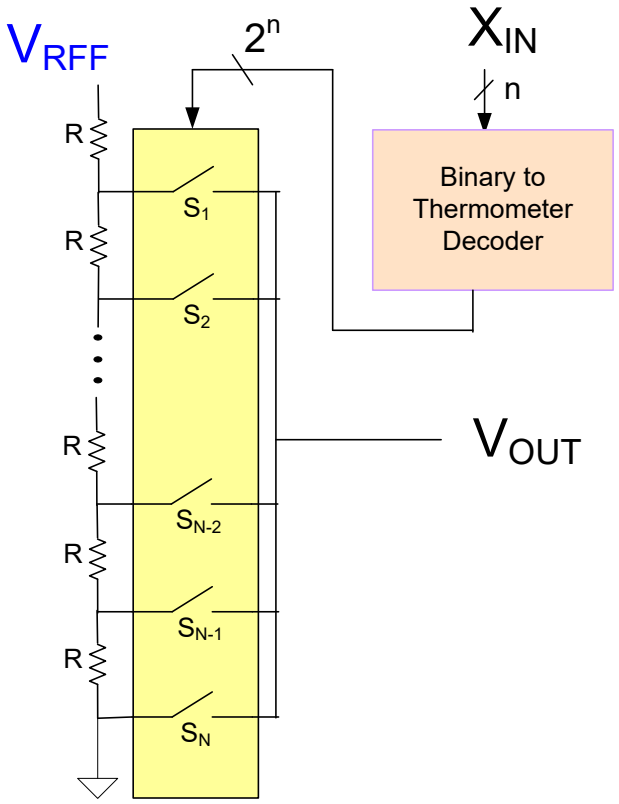
- Binary to Thermometer Decoder (BTTD) gets large for n large
- Logic delays in BTTD may degrade performance
- Matching of the resistors may not be perfect
  - Local random variations
  - Gradient effects
- How can switches be made ?



R-String DAC

Typical strategy for implementing the switch



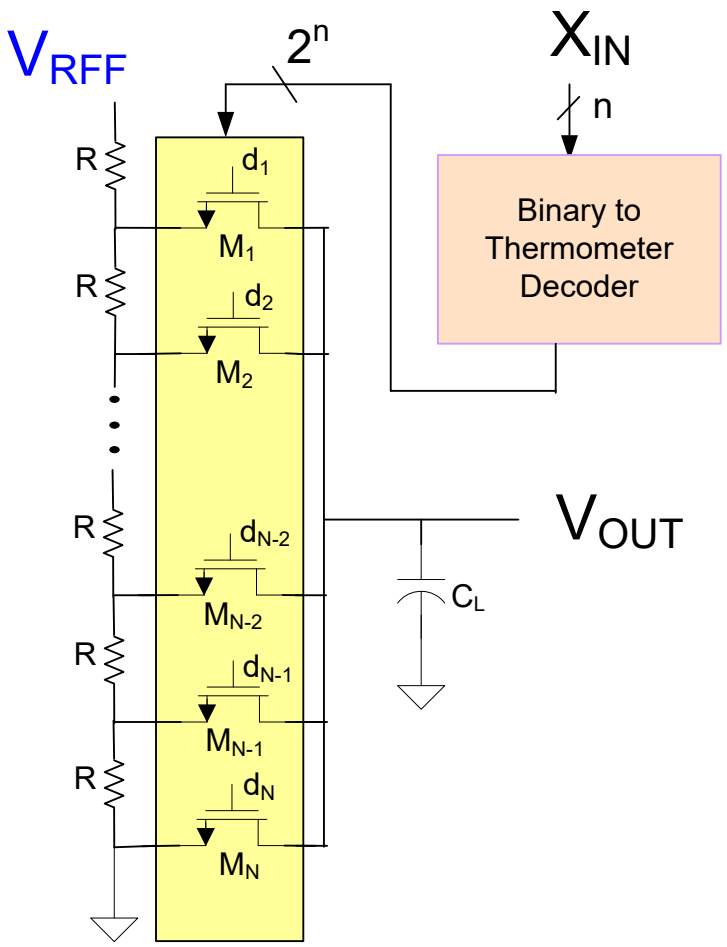


- **Switch array is an analog MUX**
- **Very simple structure**
- **Switch array combined with the BTTD forms a 2^n:1 analog MUX**

R-String DAC

R-String DAC with MOS switches

Possible Limitations:



R-String DAC

R-String DAC with MOS switches

Possible Limitations:

Switch impedance is not 0

Switch may not even turn on at all if V_{REF} is large

Switch impedance is input-code dependent

Time constants are input-code dependent

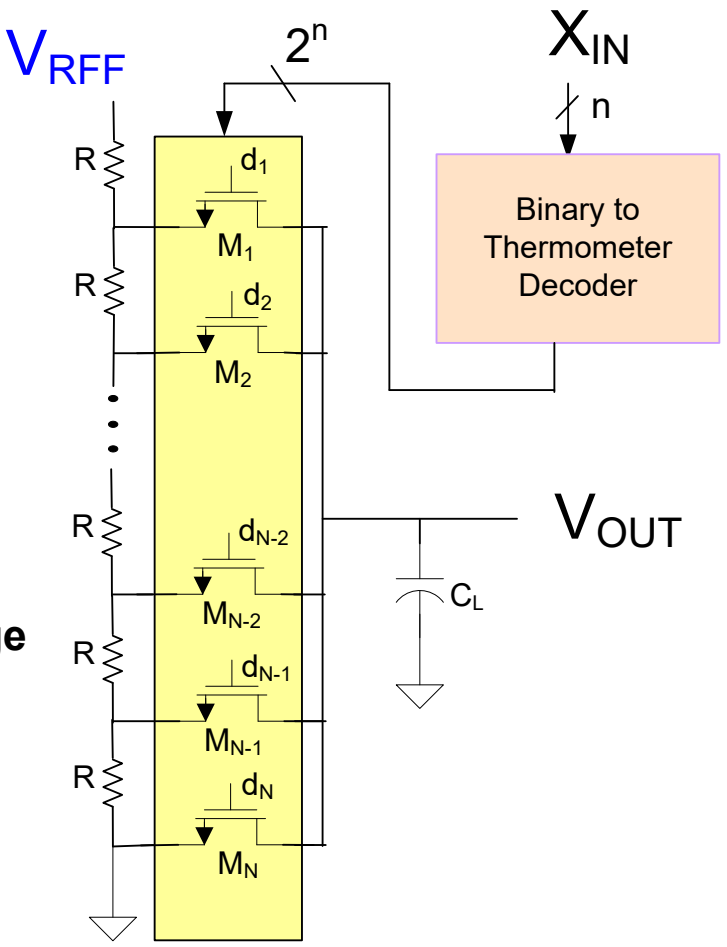
Transition times are previous-code dependent

C_L has 2^n diffusion capacitances so can get very large
(will discuss this issue next)

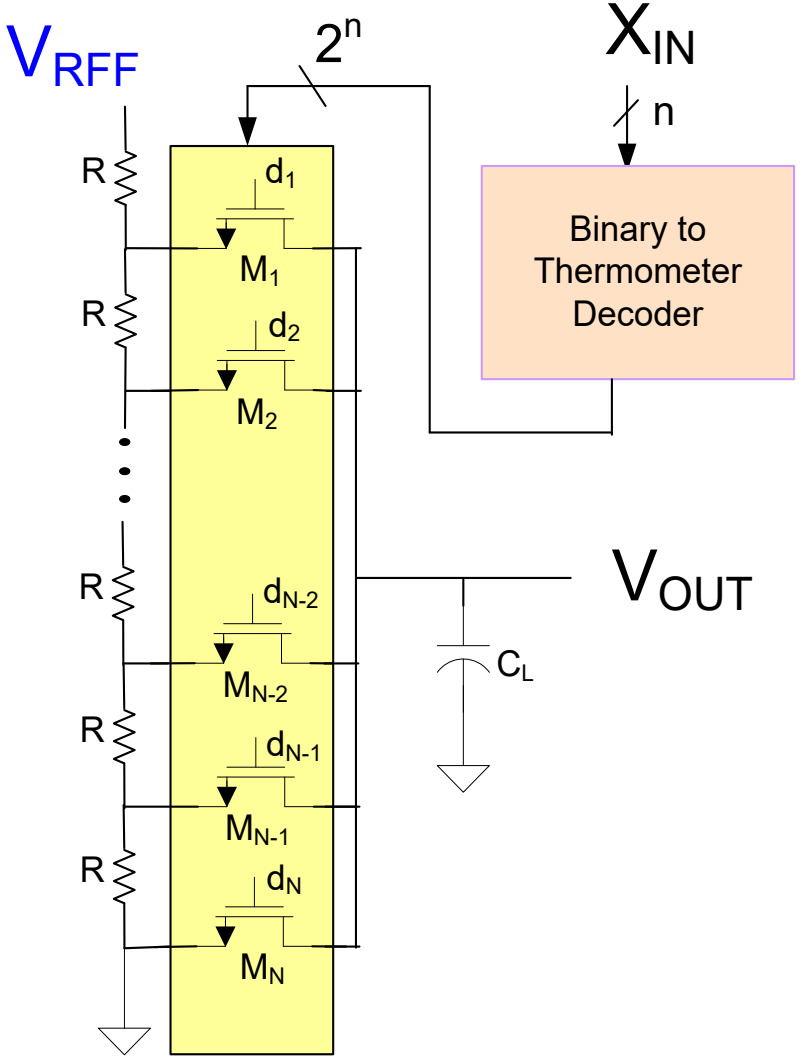
Mismatch of resistors
- **local random variation**
- **gradient effects**

Decoder can get very large for n large

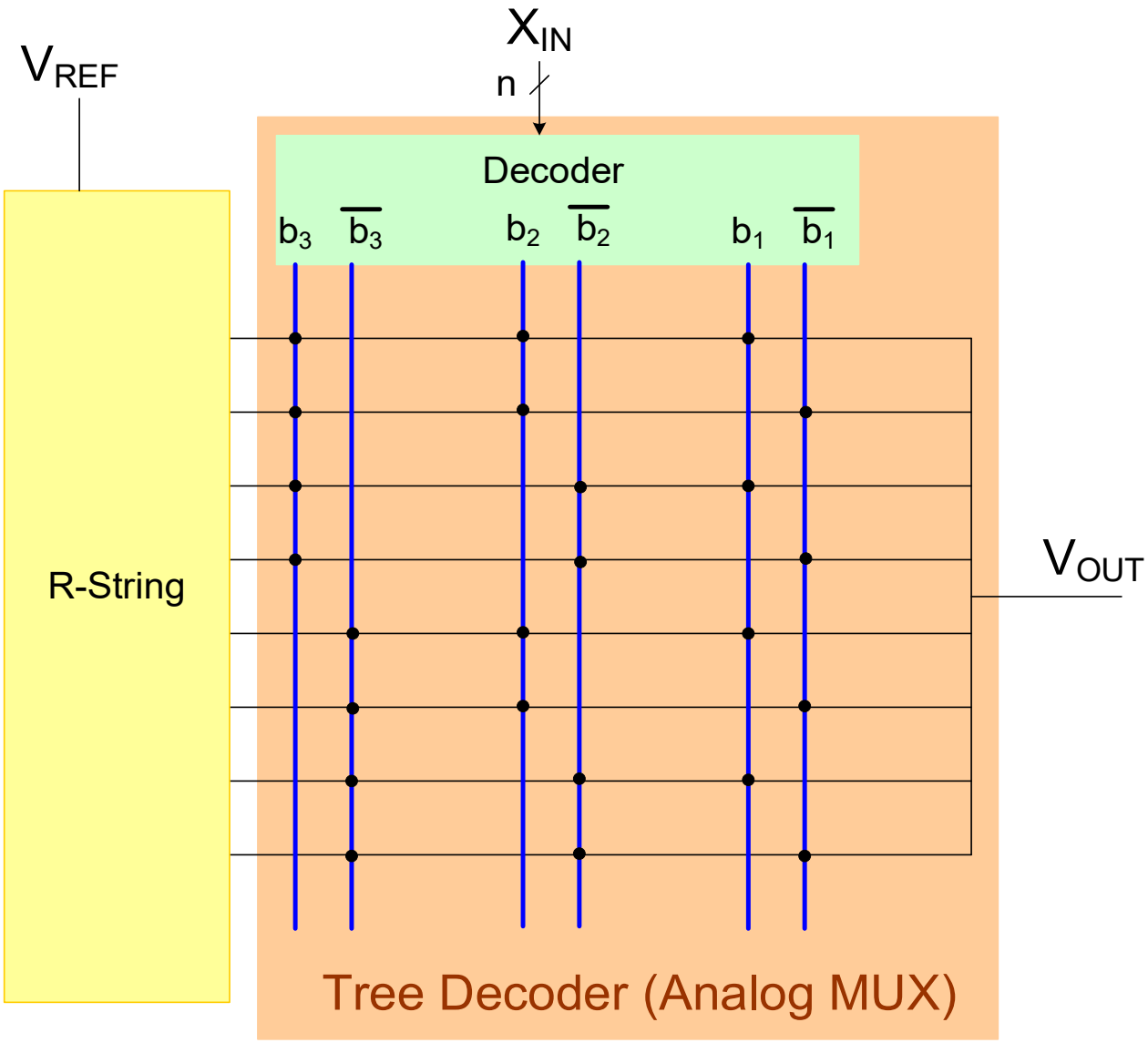
Routing of the 2^n switch signals can become very long and consume lots of area



Basic R-String DAC



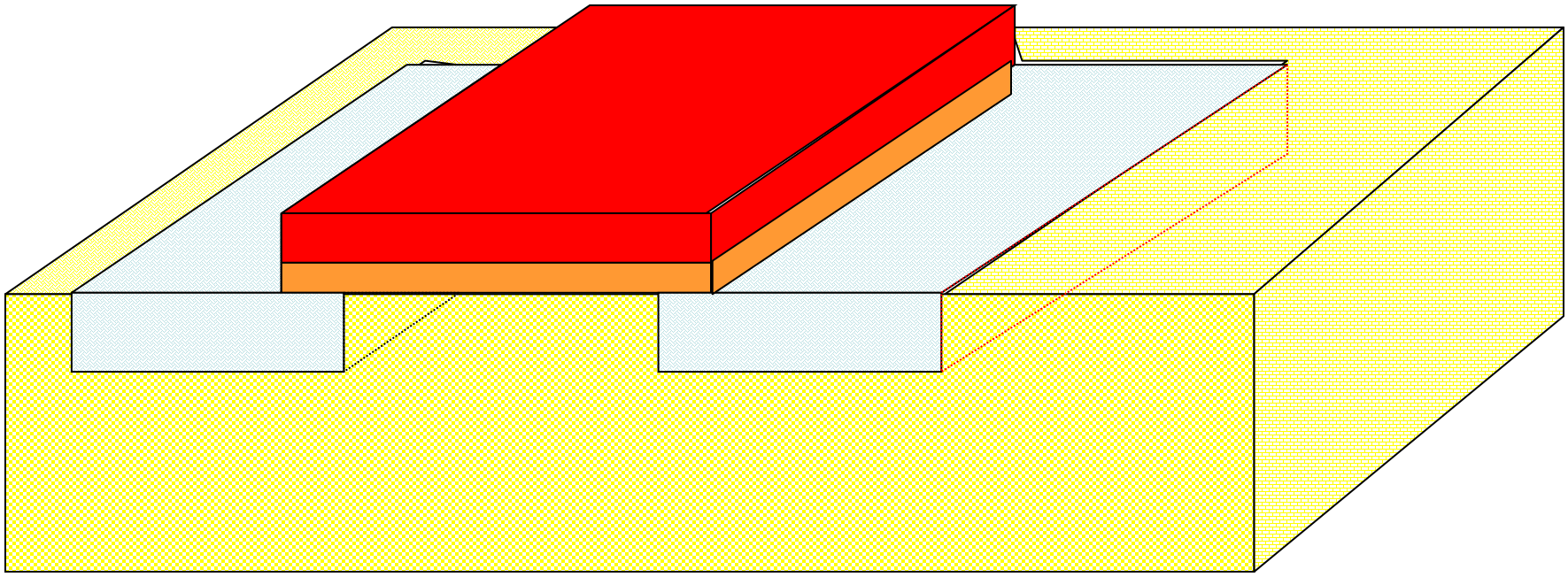
R-String DAC


V_{REF}
X_{IN}
n
Decoder
b_3
$\overline{b_3}$
b_2
$\overline{b_2}$
b_1
$\overline{b_1}$
R-String
V_{OUT}
Tree Decoder (Analog MUX)

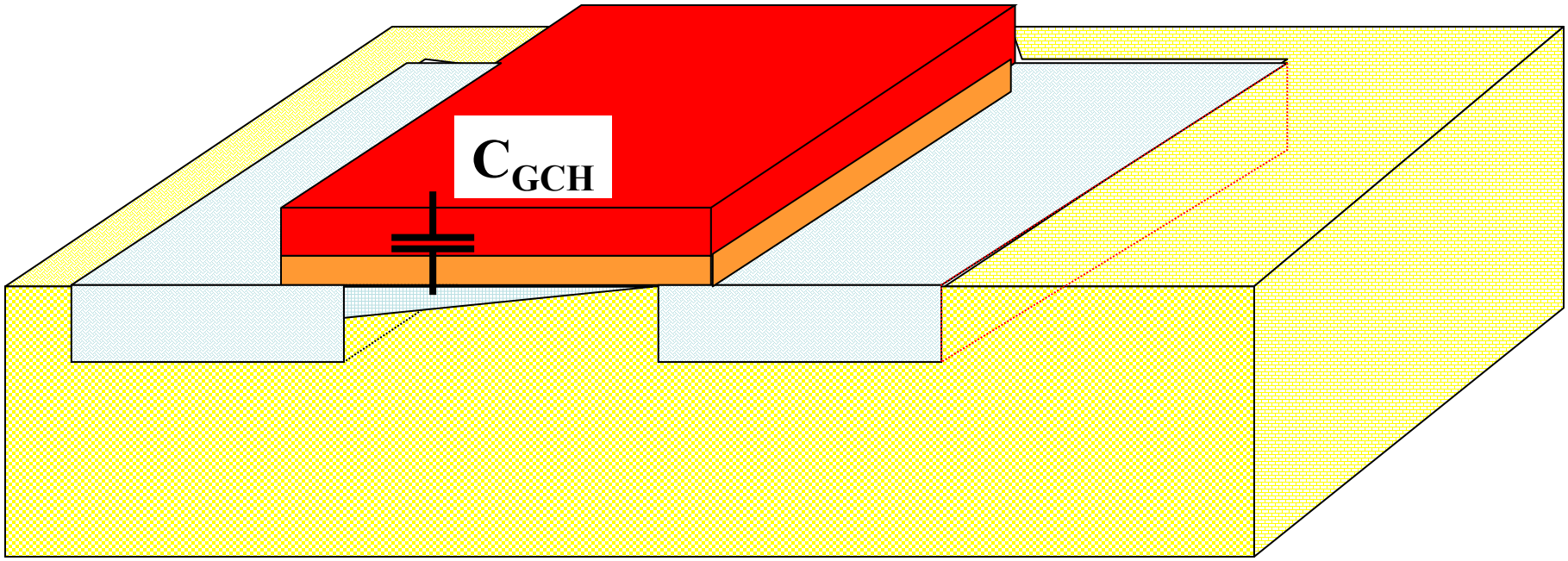
(Review from: EE 330)

Parasitic Capacitors in MOSFET

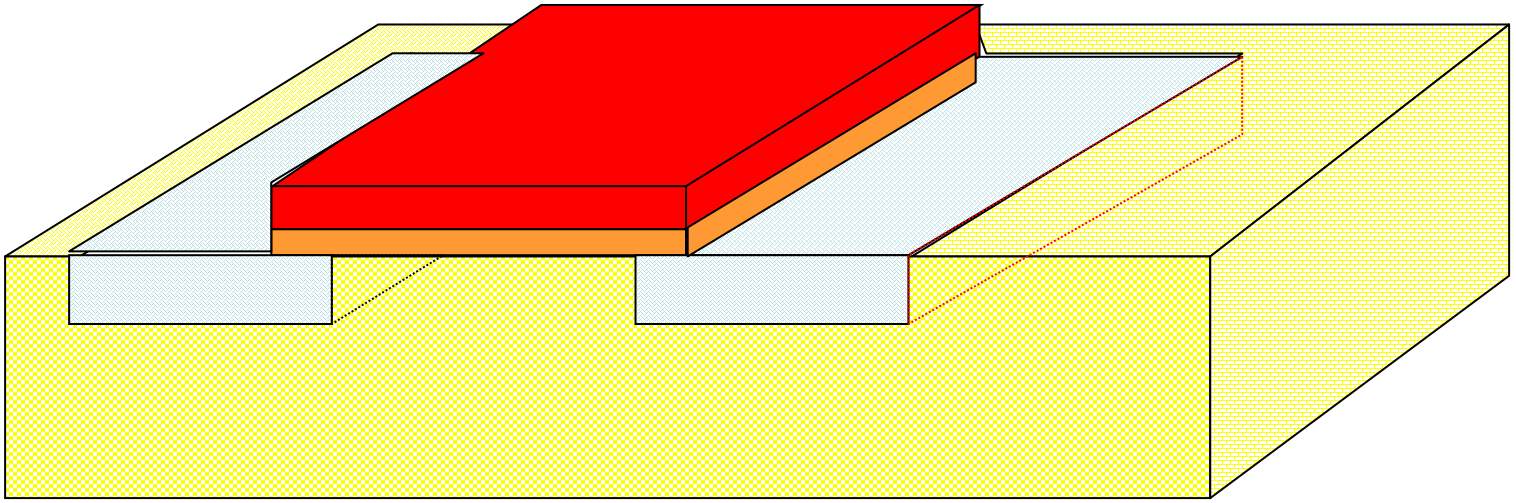
(initially assume saturation and consider two: Gate-channel and diffusion)



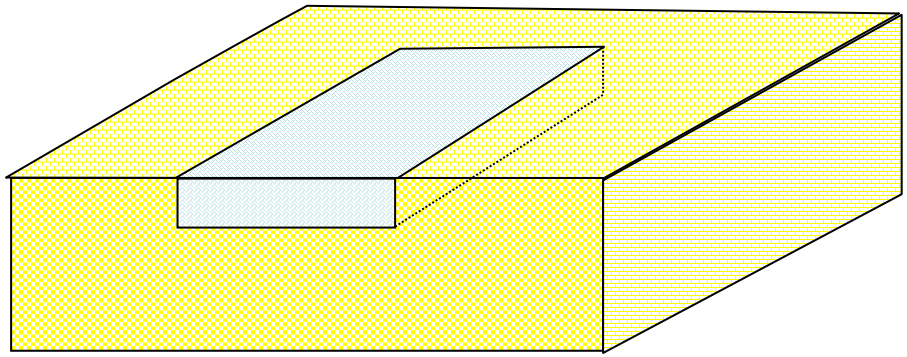
Parasitic Capacitors in MOSFET



Parasitic Capacitors in MOSFET

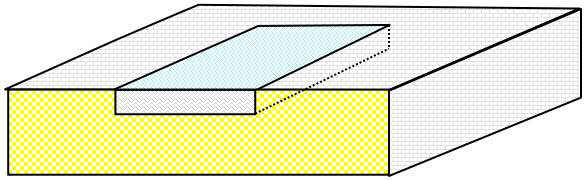


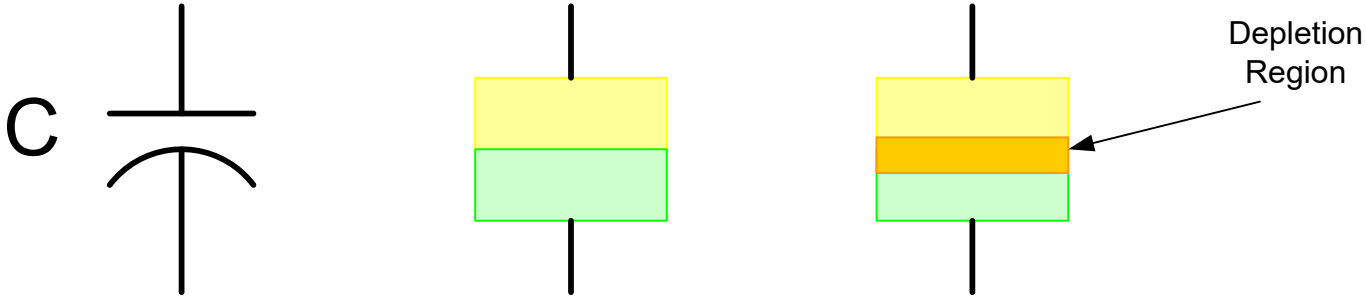
Recall that pn junctions have a depletion region!



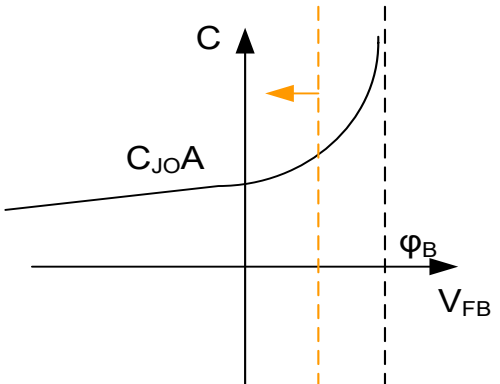
Parasitic Capacitors in MOSFET

pn junction capacitance





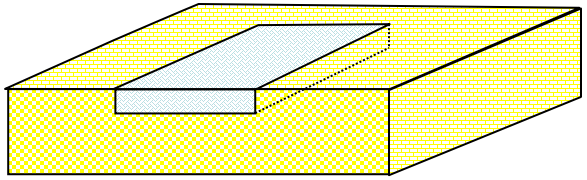
For $V_{FB}<\varphi_B/2$



$$C = \frac{C_{J0} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

Parasitic Capacitors in MOSFET

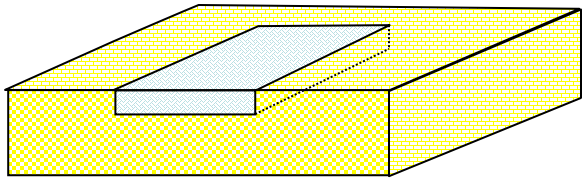
pn junction capacitance

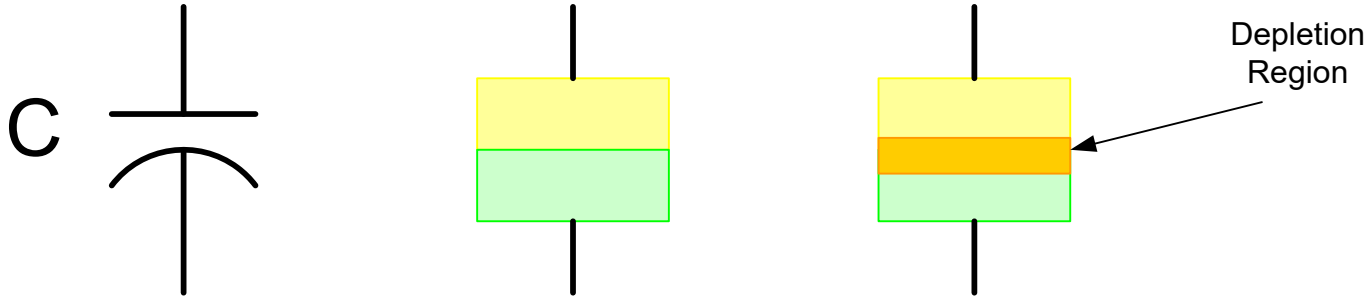


The bottom and the sidewall:

Parasitic Capacitors in MOSFET

pn junction capacitance





For a pn junction capacitor

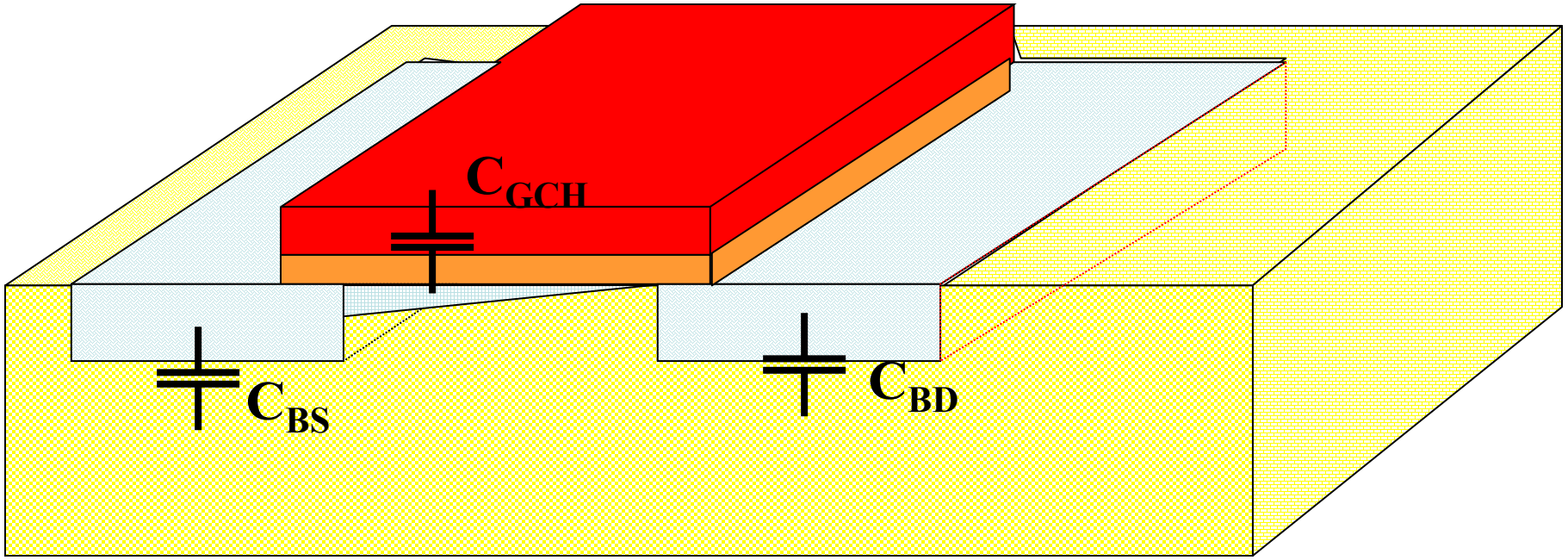
$$C_J = C_{BOT} A + C_{SW} P$$

$$C_{BOT} = \frac{C_{BOT} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

$$C_{SW} = \frac{C_{SW} P}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

Parasitic Capacitors in MOSFET

(initially assume saturation and consider two: Gate-channel and diffusion)



- Diffusion capacitances nonlinear (dependent upon voltage)
- Many more actually present
- Operating region may affect parasitics

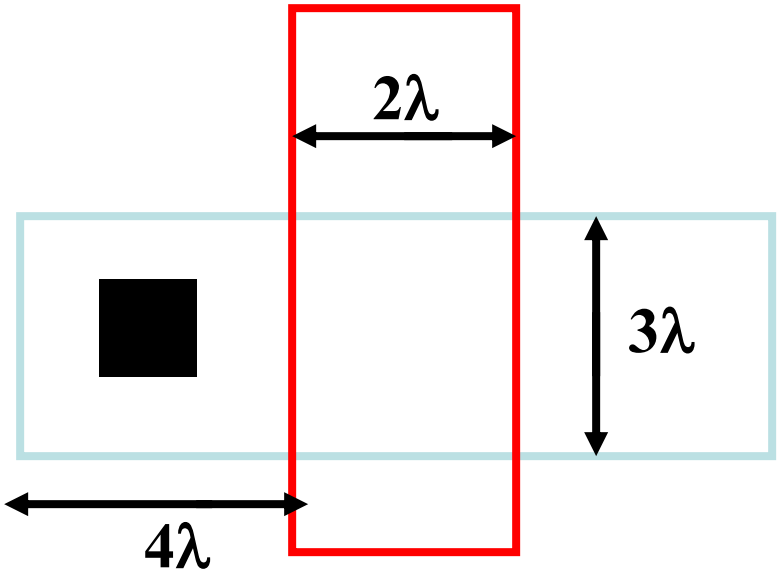
Question

- Are the parasitic capacitors relevant?

Observation

- Parasitic Capacitors are Small

Consider a minimum-sized transistor



Process Parameters from AMI 0.5u Process

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_	HR POLY2	MTL1	MTL2	UNITS
Sheet Resistance	81.5	101.9	21.6	1120	41	0.09	0.09	ohms/sq
Contact Resistance	64.6	141.9	15.8		26.8		0.8	ohms
Gate Oxide Thickness	140							angstrom

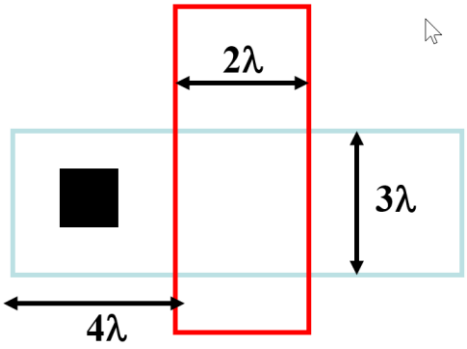
PROCESS PARAMETERS	MTL 3	N\PLY	N WELL					
Sheet Resistance	0.06	822	812					ohms/sq
Contact Resistance	0.65							ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	424	731	87		32	16	10	39	aF/um^2
Area (N+active)			2473		36	16	12		aF/um^2
Area (P+active)			2382						aF/um^2
Area (poly)				969	56	15	10		aF/um^2
Area (poly2)					50				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							39		aF/um^2
Fringe (substrate)	315	247			72	58	38		aF/um
Fringe (poly)					57	39	28		aF/um
Fringe (metal1)						48	34		aF/um
Fringe (metal2)							55		aF/um
Overlap (N+active)			195						aF/um
Overlap (P+active)			239						aF/um

λ=0.3 microns

Size of Capacitances



Gate-Channel Capacitance = $6\lambda^2$ x 2.47fF/μ^2 = 1.33fF

Source Diffusion-Substrate Capacitance =
$12\lambda^2$ x .424fF/μ^2 + 14λ x .315fF/μ =
.46fF + 1.32fF =1.78fF

Note Sidewall Capacitance larger than Bottom Capacitance

Are these negligible?

Are these negligible?

These small capacitors play the dominant role in the speed limitations of most digital circuits

These small capacitors play a major role in the performance of many linear circuits

It is essential that these capacitors (parasitic capacitors) be considered and managed when designing most integrated circuits today!

Stay Safe and Stay Healthy !

End of Lecture 31